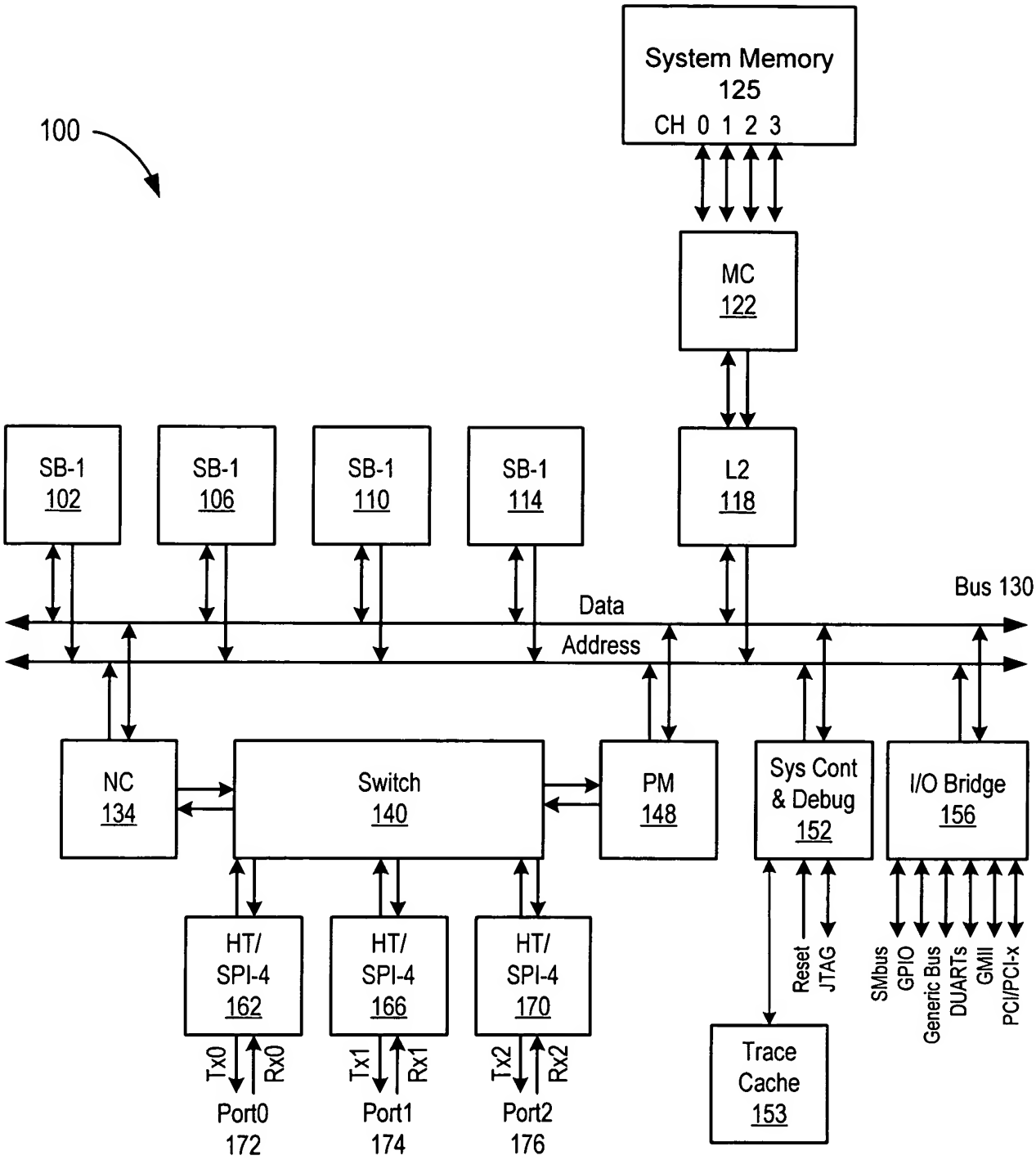
100
System Memory
125
CH 0 1 2 3
MC
122
SB-1
102
SB-1
106
SB-1
110
SB-1
114
L2
118
Bus 130
Data
Address
NC
134
Switch
140
PM
148
Sys Cont
& Debug
152
I/O Bridge
156
HT/
SPI-4
162
HT/
SPI-4
166
HT/
SPI-4
170
Tx0
Rx0
Tx1
Rx1
Tx2
Rx2
Port0
172
Port1
174
Port2
176
Trace
Cache
153
Reset
JTAG
SMbus
GPIO
Generic Bus
DUARTs
GMII
PCI/PCI-x

Figure 1

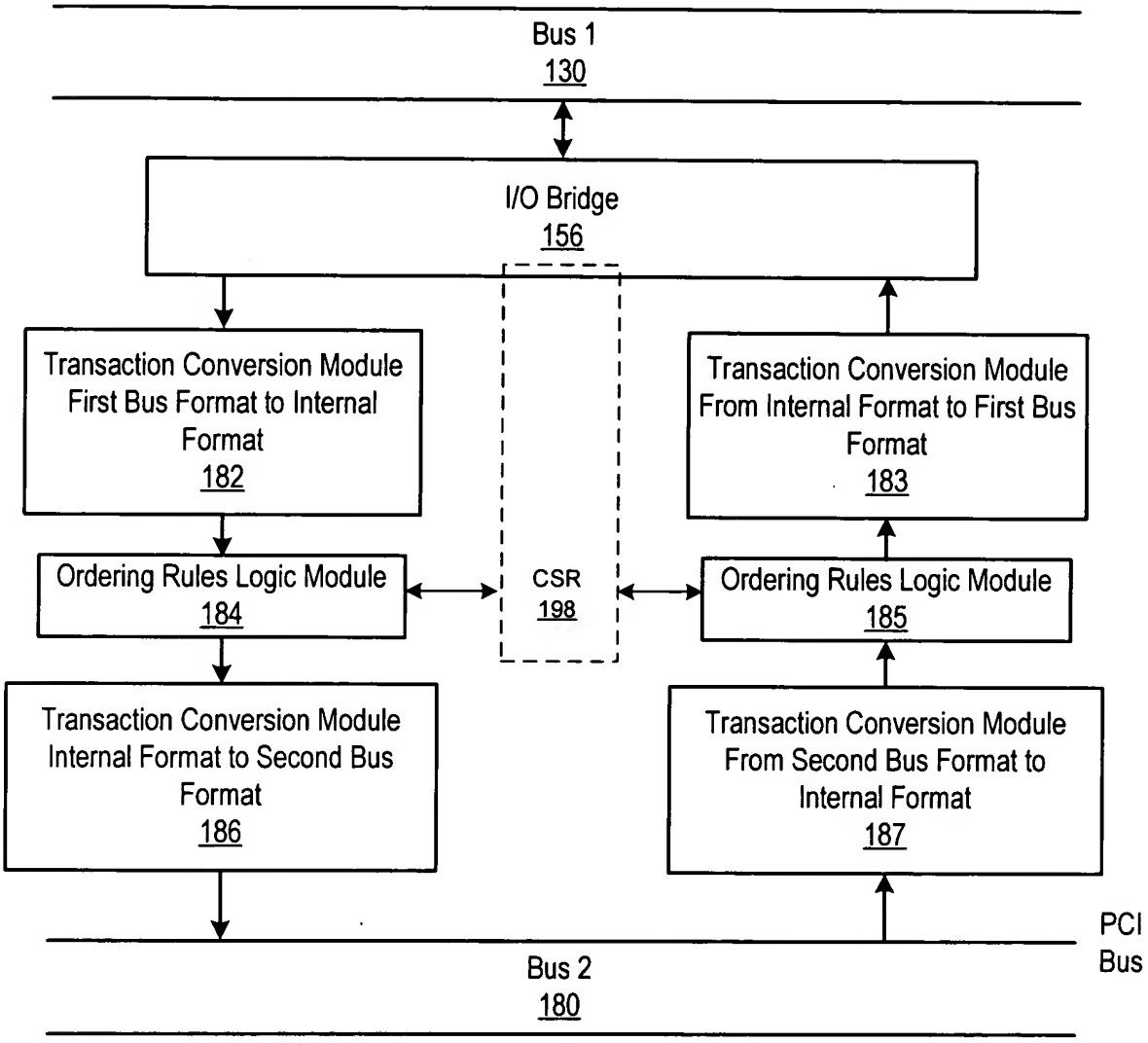
Bus 1
130
I/O Bridge
156
Transaction Conversion Module First Bus Format to Internal Format
182
Transaction Conversion Module From Internal Format to First Bus Format
183
Ordering Rules Logic Module
184
CSR
198
Ordering Rules Logic Module
185
Transaction Conversion Module Internal Format to Second Bus Format
186
Transaction Conversion Module From Second Bus Format to Internal Format
187
PCI Bus
Bus 2
180

Figure 2

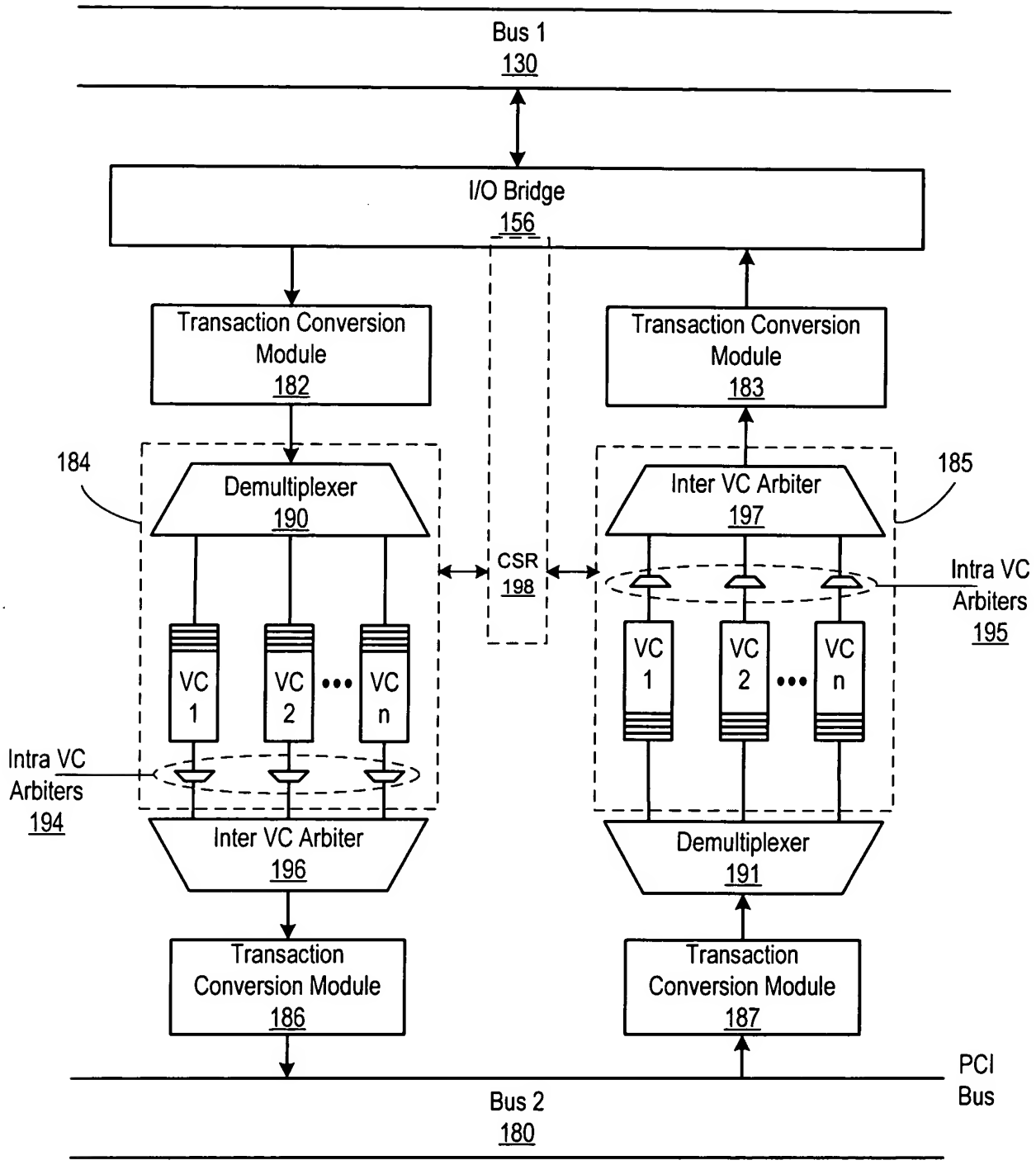
Bus 1
130
I/O Bridge
156
Transaction Conversion Module
182
Transaction Conversion Module
183
184
185
Demultiplexer
190
Inter VC Arbiter
197
CSR
198
Intra VC Arbiters
195
VC 1
VC 2
VC n
Intra VC Arbiters
194
Inter VC Arbiter
196
Demultiplexer
191
Transaction Conversion Module
186
Transaction Conversion Module
187
PCI Bus
Bus 2
180

Figure 3

	VC1	VC2	...	VCn
VC1	@	Yes	...	
VC2		@	...	
...	...	...	...	...
VCn	Yes	Yes	...	@

Figure 4

	Posted transaction	Non-posted transaction	Response
Posted transaction			
Non-posted transaction	Yes (A)		
Response	Yes (B)		

Figure 5

	C1	C2	...	Cn
C1				
C2				Yes
...				
Cn				

Figure 6

	IO command from CPU	Memory command from CPU	Memory command from Non-CPU
IO Command from CPU	Yes		
Memory command from CPU			
Memory command from Non-CPU			

Figure 7